REMARKS

In response to the Official Action mailed June 1, 2004, Applicant amends his Application and requests reconsideration. In this Amendment, no claims are added, canceled, or amended so that claims 1-5 remain pending.

The Official Action alleges that a certified copy of the priority document was not submitted because the scanned image seen by the Examiner did not include a ribbon. Submitted with this Response is a photocopy of the first page of the certified priority document that was filed, showing the presence of a ribbon. The Office routinely removes the ribbons and disassembles the priority document for scanning. Applicant requests an unqualified acknowledgement of Applicant's claim to foreign priority.

The Official Action objects to the title. Accordingly, a more descriptive title is provided.

The Official Action rejects claim 4 under 35 U.S.C. § 112, first paragraph, as not enabled by the specification. That rejection is respectfully traversed.

The Official Action contends that it is impossible to have a minus relative address in specifying a branch end because that which has already been processed cannot be skipped. Applicant respectfully submits that the rejection is a result of confusion as to the operation of the invention. The queue controller 5 of the present application uses input pointer 3 and output pointer 4 to cause some instructions to remain in the queue buffer 2. Thus, instructions preceding a BJMP may be reserved in the queue buffer 2 until after the BJMP is processed. Accordingly, those instructions preceding the BJMP are indeed not processed by the decoder until after the branch, and thus may be "skipped" (see page 15, line 22 to page 18, line 10 and Figure 4 of the patent application). Thus, the rejection is erroneous and should be withdrawn.

The Official Action rejects claims 1 and 3-5 as anticipated by Tran et al. (US Patent 5,764,946, hereinafter Tran). That rejection is respectfully traversed.

Regarding independent claim 1, Tran fails to teach all of the limitations of claim 1 for at least four reasons:

1. Tran does not teach a branch instruction that **specifies a branch end**. Tran merely discloses a conditional branch – no mention of a specified branch end is made – after which all instructions are changed to a no operation (NOOP), not just those preceding a branch end (see column 60, lines 10-17 of Tran). Thus, Tran does not teach that the instructions preceding a branch end specified by the branch instruction are processed as an operand of the branch instruction.

2. The preceding instructions of the non-existing branch end are not treated as an operand of the branch instruction. Tran specifically discloses that the instructions are changed to

a NOOP, which is not equivalent to processing the instructions as an operand of the branch instruction (see column 60, lines 10-17 of Tran). Thus, Tran does not teach that the instructions preceding a branch end specified by the branch instruction are processed as an operand of the branch instruction.

3. The changing of instructions to a NOOP is performed by the ICNXTBLK of Tran, which is a part of the instruction cache that performs way-prediction (see column 21, lines 17-34 of Tran). By contrast, claim 1 recites that the **decoder** processes all the instructions preceding a branch end as operands of the branch instruction. Thus, Tran does not teach this limitation.

4. Tran does not disclose prevention of flushing of the queue buffer of instructions as recited by claim 1. In fact, Tran teaches the exact opposite (see column 10, lines 42-55; column 82, line 63 to column 83, line 9; and column 115, lines 53-59 of Tran).

Regarding the rejection of independent claim 5, see points 1, 3, and 4 of the discussion of the errors in the rejection of claim 1.

Thus, Tran fails to teach all of the limitations of independent claim 1, its depending claims 3 and 4, and independent claim 5. Accordingly, the rejection is erroneous and should be withdrawn.

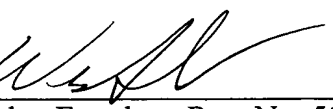
The Official Action rejected claim 2 as unpatentable over Tran in view of Breeding (Microprocessor System Design Fundamentals). That rejection is respectfully traversed.

The propriety of the rejection of claim 2 relies on the assertion that Tran teaches all of the limitations of claim 1, which are incorporated into claim 2. As discussed above, that assertion is erroneous. Accordingly, the rejection of claim 2 is also erroneous, and should be withdrawn.

Since no claim has been amended in response to the Official Action, any new rejection based upon newly applied prior art or a different legal ground cannot properly be a final rejection.

Prompt allowance of claims 1-5 is earnestly solicited.

Respectfully submitted,



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